Thin and flexible CMOS Image Sensors

J. Häfner

haefner@iwe1.rwth-aachen.de

CCD and CMOS image sensors today are widely used in many application areas including consumer and industrial cameras, cellular phones and medical devices. Those sensors are as most integrated circuits around 750 µm thick and therefore rigid and brittle. As a consequence, the sensors are always flat and cannot be inserted into cavities which are only accessible by small openings. However, when silicon is thinned down to 30 µm it becomes flexible and can be bent. This offers the possibility to wrap the sensor around a rod and to gather 360° images.

Thin silicon has gained increasing attention in recent years. In smart card and RF-ID tags chips with a reduced thickness are used because of the limited space available and because thinner silicon can better withstand bending [1]. When the silicon thickness is reduced to 20 µm a bending radius of 10 mm is easily achievable (Fig. 1). Other applications include power semiconductors where thinning reduces series resistances and thereby ohmic losses [2] and 3D stacked memory chips which enhances storage capability per area [3].

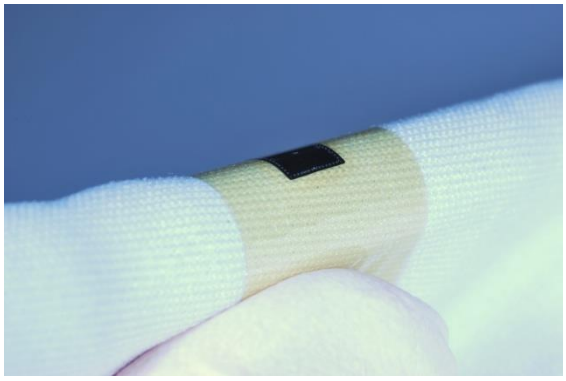

Fig. 1: *Thin silicon dummy chip embedded in polyimide foil and wrapped around a pen.*

The goal of this project is to investigate the optical and electrical properties of CMOS integrated image sensors on thinned single crystalline silicon substrates. Therefore, the influence of mechanical stress caused by bending on the optical characteristics (spectral sensitivity, quantum efficiency, dark current) of photosensors and photosensor arrays and the electrical characteristics (threshold voltage, carrier mobility, leakage current) of passive and active devices shall be examined. Finally, based on the findings in the previous experiments, concepts and design rules shall be developed that minimize the effect of mechanical stress on the device performance.

For investigating the influence of mechanical stress on those devices a test chip (Fig. 2) has been designed and manufactured in a 0.35 µm CMOS process. It contains photodiodes, transistors, differential amplifiers and capacitors in different orientations relative to the silicon crystal planes.

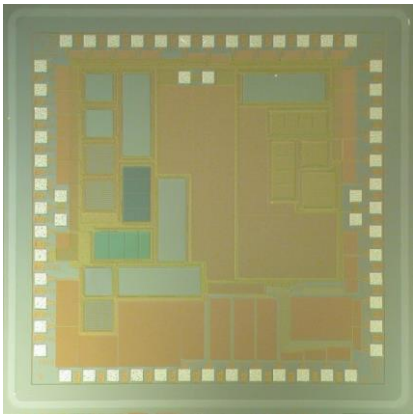

Fig. 2: *Test chip containing photodiodes, transistors, differential amplifiers and capacitors in different orientations.*

For chip separation the Dicing-by-Thinning (Fig. 3) approach is chosen because it causes less damage to the chip edges than conventional sawing and thereby enhances chip robustness [~~1~~4]. Trenches are etched on the front side of the silicon wafer containing the test chips that will later define the chip boundaries (Fig. 3b). After attaching the silicon to a carrier substrate (Fig. 3c) material is removed from the backside until the trenches open up and the chip is separated from the surrounding silicon (Fig. 3d). Finally the thin chip can be detached from the carrier substrate (Fig. 3e).

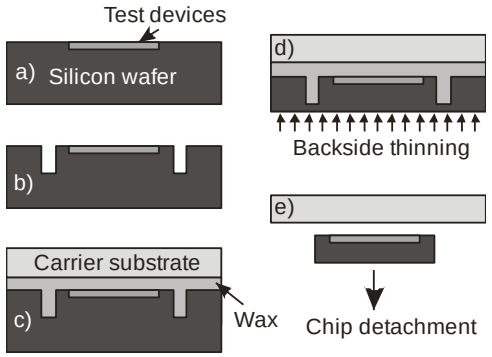

Fig. 3: *Dicing by thinning concept. a) silicon wafer with test chip; b) plasma trench etching; c) attaching to carrier substrate; d) backside thinning and chip separation; e) chip detachment*

Acknowledgements This work is supported by the German Research Foundation (DFG) under grant “FlexBild”.

Projectpartners

- Universität Duisburg-Essen, Fachgebiet Elektronische Bauelemente und Schaltungen
  http://www.uni-due.de/ebs/

- Fraunhofer-Institut für Mikroelektronische Schaltungen und Systeme
  http://www.ims.fraunhofer.de

[1] R. Decker et al., “A 10 µm Thick RF-ID Tag for Chip-in-Paper Applications”, Proc. IEEE Bipolar/BiCMOS Circuits and Technology meeting (BCTM), Santa Barbara, California, USA, p 268, October 9-11, 2005

[2] D. Graovac, A. Christmann, M. Miinzer, “Power semiconductors for hybrid and electric vehicles”, Power Electronics and ECCE Asia (ICPE & ECCE), 2011 IEEE 8th International Conference on, pp.1666-1673, May 30-June 3, 2011

[3] M. Kawano et al., “A 3D Packaging Technology for 4 Gbit Stacked DRAM with 3 Gbps Data Transfer”, Electron Devices Meeting, 2006 pp.1-4, December 11-13, 2006

[~~1~~4] K. Hungar, W. Mokwa, "Gold/tin soldering of flexible silicon chips onto polymer tapes", Journal of Micromechanical Engineering, Vol. 18, No. 6, 2008